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CLAIMS

What is claimed is:

A receive descrializer circuit which frames data, comprising:

a sampling flip flop for receiving serial data including a data reference pattern, wherein said sampling flip flop retimes said serial data to a recovered clock as sampled serial data;

a demultiplexer for deserializing said sampled serial data into a parallel data word timed to a word clock from a clock generator;

a comparator for making a comparison of said parallel data word with a preset data reference pattern until said/comparison results in a match;

a logic controller for interpreting whether the output of said comparator results in said match and for generating a shift pulse following each of said comparisons which do not result in said match; and

said clock generator for dividing said recovered clock into phase clocks, said word clock being one of said phase clocks, and for disabling said phase clocks for a period of one bit upon receipt of said shift pulse, thereby creating a one bit shift in the alignment of said parallel data word being generated on said word clock by said demultiplexer.

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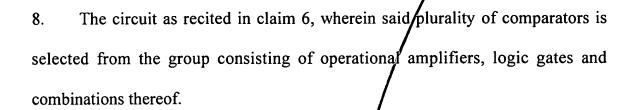
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- 2. The circuit as recited in claim 1, wherein said recovered clock is a local clock whose negative edge is pre-aligned with the transition edge of said serial data by a clock recovery module.
- 5 3. The circuit as recited in claim 1, wherein said recovered clock is the source clock for said phase clocks.
 - 4. The circuit as recited in claim 1, wherein said preset data reference pattern is derived from a plurality of hard-wired connections.
 - 5. The circuit as recited in claim 1, wherein said preset data reference pattern is derived from data received from a transmitter upon initialization of said circuit.
 - 6. The circuit as recited in claim 1, wherein said comparator is a plurality of comparators whose outputs are combined by said logic controller to determine whether said comparator results in said match.
 - 7. The circuit as recited in claim 6, wherein each of said plurality of comparators has a first and second input, said first input driven by a separate reference bit from said preset data reference pattern and said second input driven by a separate sample bit from said parallel data word.

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and



- 5 9. The circuit as recited in claim 6, wherein said plurality of comparators is eight exclusive OR logic gates.
 - 10. A method of framing data in a receive descrializer circuit, comprising the steps of:

receiving serial data including a data reference pattern from a transmitter; retiming said serial data to a recovered clock as sampled serial data;

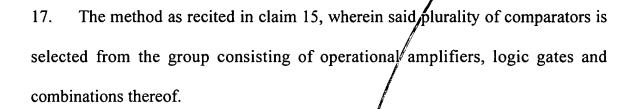
descrializing said sampled serial data into a parallel data word timed to a word clock;

comparing said parallel data word with a preset data reference pattern until a match results;

generating a shift pulse when said comparing does not result in said match; dividing said recovered clock into phase clocks, including said word clock;

disabling said phase clocks for one bit period each time said shift pulse is
generated, thereby creating a one bit shift in the alignment of said parallel data
word being generated on said word clock in said demultiplexer.

- 11. The method as recited in claim 10, wherein said recovered clock is a local clock whose negative edge is pre-aligned with the transition edge of said serial data by a clock recovery module.
- 5 12. The method as recited in claim 10, wherein said recovered clock is the source clock for said phase clocks.
 - 13. The method as recited in claim 1/0, wherein said preset data reference pattern is derived from a plurality of hard wired connections.
 - 14. The method as recited in claim 10, wherein said preset data reference pattern is derived from data received from a transmitter upon initialization of said receive describing receive describing a transmitter upon initialization of said received describing a transmitter upon a transmi
- 15. The method as recited in claim 10, wherein said comparator is a plurality of comparators whose outputs are combined by said logic controller to determine whether said comparator results in said match.
- 16. The method as recited in claim 15, wherein each of said plurality of comparators has a first and second input, said first input driven by a separate reference bit from said preset data reference pattern and said second input driven by a separate sample bit from said parallel data word.



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- 18. The method as recited in claim 15, wherein said plurality of comparators is eight exclusive OR logic gates.
- 19. A method of framing data in a receive descrializer circuit, comprising the steps of:

receiving serial data;

generating a local clock based on said serial data;

deserializing said serial data into a parallel data word;

comparing a portion of said/parallel data word with a preset data reference

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adjusting said local clock to an adjusted local clock based on the results of said comparing; and

timing subsequent data to said adjusted local clock.

